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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,023	10/19/2001	Chang Rock Song	054216-5003	7126

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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,023	SONG, CHANG ROCK	
	Examiner	Art Unit	
	Suk-San Foong	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "said first Ruthenium electrode" in line 18. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 1, line 24, it appears that "a" should be replaced by--said--; unless another step is intended.

6. Claim 16, it is questioned whether the "silicon oxide film" is the "interlayer insulating layer".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 11, 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605).

Okuno et al. teach a method of forming a capacitor in semiconductor devices which includes forming silicon oxide layer 201 over silicon substrate 200 (Col. 9, lines 56-59, and Fig. 6A), then forming nitride film 202 on silicon oxide layer 201 (Col. 9, lines 60-62), etching through nitride film 202 and silicon oxide film 201 to form contact hole 203 (Col. 9, line 64 to Col. 10, line 3, and Fig. 6B), then depositing polysilicon layer 204 over substrate 200 thereby filling contact hole 203 (Col. 10, lines 4-11, and Fig. 6C), subsequently performing etch back process to remove upper portion of polysilicon layer 204 and leaving remaining portion of polysilicon layer 204 in contact hole 203 (Col. 10, lines 12-15, and Fig. 6D), then forming ohmic

contact layer 206 such as cobalt silicide by first depositing cobalt film 204 over substrate 200 and contact hole 203, then performing heat treatment to form the cobalt silicide layer (Col. 10, lines 16-20, and Fig. 7A) and removing unreacted portion of cobalt film (Col. 10, lines 29-30, and Fig. 7C), subsequently depositing anti-diffusion film 207 such as TiN on ohmic contact layer 206 by first depositing TiN film over substrate 200 and removing portion of TiN film using chemical mechanical polishing method (Col. 10, lines 31-41, and Figs. 7C and 8A), subsequently depositing insulating film 210 such as silicon oxide over entire surface of substrate 200 including anti-diffusion film 207 (Col. 10, lines 47-49, and Fig. 8B), then etching a portion of insulating film 20 to form concave hole 212 with internal wall (Col. 10, lines 52-60, and Fig. 8C), subsequently forming first electrode 216 by first depositing conductive film 213 such as platinum film or ruthenium (Col. 14, lines 1-3) on entire surface of substrate 200 and removing portions of conductive film 213 not formed on the internal wall of concave hole 212 (Col. 11, lines 1-5 and 25-30, and Figs. 9A-9C, and 10A), subsequently forming BST dielectric film 217 on first electrode 216 (Col. 11, lines 49-52, and Fig. 10B), then depositing platinum film over BST dielectric film 217 to form second electrode 218 (Col. 11, lines 53-55, and Fig. 10C), and consequently forming capacitor 219 comprised of first electrode 216, BST dielectric film 217 and second electrode 218 (Col. 11, lines 55-59).

Okuno et al. do not disclose the step as recited in claim 1, lines 7-8.

Lou discloses a method of forming a capacitor over contact hole which includes forming insulating layer 103 over substrate 101 (Col. 2, lines 13-14, and Fig. 1), then forming silicon nitride layer 105 over insulating layer 103 (Col. 2, lines 14-16), then forming contact hole 107 though layers 103 and 105 (Col. 2, lines 16-19), subsequently depositing conductive material

such as doped polysilicon in contact hole 107 (Col. 2, line 20-24), then removing portions of conductive layer (Col. 2, lines 24-26), then forming insulating layer 109 (Col. 2, lines 28-30), subsequently forming opening 111 in insulating layer 109 (Col. 2, lines 32-34, and Fig. 2), and then forming bottom electrode layer 113, dielectric layer 119 and top electrode 121 (Col. 3, line 58 to Col. 4, line 5).

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable formation of conductive or doped polysilicon film in the process of Okuno et al. to be performed.

The combination of Okuno et al. and Lou do not disclose forming interlayer insulating film comprised of silicate glass material such as PSG and USG.

The combination of Okuno et al. and Lou do not disclose performing NH_3 plasma process and N_2O plasma process prior to depositing BST dielectric film.

Yang et al. teach a method of forming capacitor on semiconductor devices which includes forming insulating layer 235 comprised of materials such as BPSG and phosphorous-doped silicon oxide over substrate 205 (Paragraph [0036], and Fig. 2B), then etching insulating layer 235 to form contact hole (Paragraph [0037], and Fig. 2C), subsequently forming ohmic contact layer 240 (Paragraph [0038], and Fig. 2D), then forming first electrode 235 comprised of material such as ruthenium (Paragraph [0039], and Fig. 2E) by chemical vapor deposition method (Paragraph [0040]), subsequently performing plasma process in ambients containing NH_3 and N_2O and, thus, forming barrier layer 250 (Paragraph [0047], and Fig. 2F), then forming BST dielectric film 255 over first electrode 235 (Paragraph [0049]), subsequently annealing BST dielectric film (Paragraph [0050], and Fig. 2G), and forming second electrode 260 such as

ruthenium by chemical vapor deposition method on BST dielectric film 255 (Paragraph [0055], and Fig. 2I).

It would have been within the scope to one ordinary skill in the art to combine the teachings Yang with the combination process to enable the step of forming insulating film 20 of Okuno et al. to be performed.

In view of both NH_3 and N_2O ambients are suitable for the entire step of forming the barrier layer, it would have been within the scope to one ordinary skill in the art to combine both teachings to employ NH_3 plasma to enable a portion of the step to be performed and employ N_2O plasma to enable performing a remaining portion of the step to be performed to achieve a desired thickness and properties of the barrier layer (See MPEP 2144.04 V (C)).

The combination process does not disclose crystallizing BST dielectric film through rapid thermal process.

The combination process does not disclose performing a thermal treatment to stabilize said capacitor.

In regard to claim 11, the combination process does not disclose depositing the BST dielectric film by chemical vapor deposition method and the thickess of about 150 to 500 Å.

Iizuka teaches a method of forming a capacitor for a semiconductor device which includes forming lower electrode 28 comprised of materials such as ruthenium and platinum (Col. 3, lines 35-40), then forming BST dielectric film 30 by ECR-chemical vapor deposition method to a thickness of 200Å over lower electrode 28 (Col. 3, lines 41-42), subsequently performing rapid thermal process at a temperature of 300 to 400°C for about 40 minutes to crystallize BST dielectric film 30 (Col. 4, lines 56-59), then forming upper electrode 32

comprised of materials such as ruthenium and platinum (Col. 3, lines 35-40), and performing thermal treatment after forming the capacitor in a gas mixture of oxygen and nitrogen at a temperature of 300 to 400°C (Col. 49-52).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Iizuka and the combination process teachings because it would enable formation of BST dielectric film 217 of Okuno et al. to be performed and obtain further advantage of suppressing leak current (Iizuka, Col. 4, lines 60-64).

With respect to claim 11, note that the disclosed thickness of the BST dielectric film is within the recited range.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Iizuka and the combination process because it would enable formation capacitor 219 of Okuno et al. to be performed and obtain further advantage of improving the crystallization of the boundary between top electrode and BST dielectric film and reducing leak current at room temperature (Iizuka, Col. 6, lines 1-6).

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13, 14 and 16 above.

In regard to claim 2, the combination process does not disclose the recited thickness of the nitride film.

It would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to

choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

10. Claims 3, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13 and 14 above, and further in view of Graettinger et al. ('709).

The combination process does not disclose the steps as recited in claim 3 and 4.

The combination process does not disclose the recited thickness of the anti-diffusion film and the deposition method such as physical vapor deposition or chemical vapor deposition.

Graettinger et al. disclose a method of forming a capacitor for semiconductor devices which includes forming contact hole 200 through insulating layer 150 (Col. 4, lines 43-45, and Fig. 2), then depositing conductive material 500 such as polysilicon through chemical vapor deposition in contact hole 200 (Col. 5, lines 30-35, and Fig. 5), then etching back conductive material 500 (Col. 5, lines 42-50, and Fig. 6), subsequently depositing anti-diffusion film 700 such as TiN or TiAlN using chemical vapor deposition method (Col. 5, lines 51-59, and Fig. 7),

then depositing insulating layer 940 over substrate 110 and forming concave hole in insulating layer 940 (Col. 6, lines 30-31, and Fig. 9), then depositing bottom electrode 910 (Col. 6, lines 29-30), then depositing BST dielectric film 920 over bottom electrode 910 (Col. 6, lines 33-46), and depositing top electrode 930 over BST dielectric film 920 (Col. 6, lines 29-31).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Graettinger et al. with the combination process because it would enable formation of the doped polysilicon layer of the combination to be performed.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Graettinger et al. with the combination process because it would enable formation of anti-diffusion film 207 of Okuno et al. to be performed and obtain further advantage of preventing dopant diffusion (Graettinger et al., Col. 6, lines 1-9).

The combination process does not disclose the recited thickness of the doped polysilicon layer and the depth of the etch-back process.

The choice of thickness of the doped polysilicon and the depth of the etch-back process would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

The combination process does not disclose the recited thickness of the anti-diffusion film.

The choice of thickness of the anti-diffusion film would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13, 14 and 16 above.

The combination process does not disclose the thickness of the ohmic contact layer 206 as recited.

The choice of thickness of the ohmic contact layer would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13, 14 and 16 above.

The combination process does not disclose the thickness of the interlayer insulating film as recited.

The choice of thickness of interlayer insulating film would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

13. Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13, 14 and 16 above.

The combination process does not disclose the thickness of first electrode 216 as recited in claim 8.

The combination process does not disclose the thickness of second electrode 218 as recited in claim 14.

The choice of thickness of the conductive film 213 and would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

14. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13, 14 and 16 above.

The combination process does not disclose the steps recited in claims 9 and 10.

One of ordinary skill in the art would have been motivated to arrive at selected power, pressure, flow rate and temperature for use in the process of the combination through routine experimentation depending on the desired device dimension and device characteristics because power, pressure, flow rate and temperature are recognized to be result effective variables.

15. Claims 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. ('262) in combination with Yang et al. ('334), Iizuka ('996) and Lou ('605) as applied to claims 1, 11, 13, 14 and 16 above.

In regard to claim 12, the combination process does not disclose the recited temperature and duration for the rapid thermal process.

In regard to claim 15, the combination process does not disclose the recited temperature and duration for the thermal treatment step

One of ordinary skill in the art would have been motivated to arrive at selected power, pressure, flow rate and temperature for use in the process of the combination through routine experimentation depending on the desired device dimension and device characteristics because power, pressure, flow rate and temperature are recognized to be result effective variables.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

GF
October 20, 2002

George Fourson
Primary Examiner
Art Unit 2823